A Circuit Board Test Technology by Integrating Multifunctional Digital Logic Circuits into the CPLD Chip

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Abstract: This paper proposes a circuit board functional test technique with integrating multifunctional digital logic circuits into the integrated chip (IC) for troubleshooting the circuit board in advance. The proposed technique integrates four digital logic circuits into the CPLD chip to detect and confirm that the input and the output devices of the circuit board can work properly. The input devices include clocks, dip switches and push buttons; the output devices include the buzzer, LEDs and 7-segment displays. The designed multifunctional IC chip is experimented by using EPM7064SLC44-10 CPLD based commercial peripheral board and utilizing Altera Quartus II software tool for the circuit compiling, simulating, floor-planning and programming processes. According to the experimental results, the proposed approach is an effective educational tool which can be used to check the input and the output devices of the circuit boards, demonstrate the multifunctional IC design skills at the beginning of the practical training course, enhance the teaching quality and increase the learning effects.
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Keywords: Circuit board; functional test; digital logic circuits; integrated chip; CPLD.

1. Introduction

With promoted diversity education, an institution has developed various learning education such as distance learning, on-line learning and adult learning as well as undergraduate, graduate and doctoral programs. Of all these learning education, if the learners cannot initially learn the educational resources in an efficient manner, they will not retain them well. Therefore, it is necessary to supply various available curriculum materials such as providing practical training materials to help learners retaining what the course delivers to them effectively. The literatures (Abedi and Badragheh, 2011) specifically suggested that the adult education needs a variety of practical resources to reinforce the skill and hold the key learning.

Digital logic circuit design in colleges usually is an important and fundamental subject because it is the basis for students developing the mechanical/electrical controls, embedding system designs, and microcontroller related applications. In reviewing some researches related to adopting Complex Programmable Logic Device (CPLD) in developing specific customized autonomous products, the study (Tsai and Chen, 2002) designed a decoder/counter integrated circuit (IC) for motor control. The research (Ali and Kshirsagar, 2010) developed an open loop stepper motor controller. The reference (Samman and Syarnsuddin, 2002) introduced the programmable fuzzy logic controller. The literature (Tsai et al., 2004) designed a digital programmable control IC for common-neutral half-bridge bilateral AC-DC-AC Converters. The study (Shih et al., 2011) proposed a programmable system-on-chip (PSoC) technology to prevent unauthorized users from abusing or disclosing computerized personal data during transit and at rest. In addition, two institutes, Bureau of Taiwan Labor Vocational Training Council (TVTC) and Taiwan Embedded Microcontroller Development Institution (TEMI), have provided digital logic circuit design technical skill verifications and issued related certifications, respectively. Both institutes adopt different CPLD based commercial boards for the practical training and authentication. The book (Liu, 2017) introduced and explicated the examination questions of B level capability certification on digital electronics skill authentication. The author also published two books (Chao, 2013) which explicated every examination questions of the practical and professional level capability certifications on digital logic circuit design.

In reviewing some references related to utilizing CPLD based commercial peripheral boards in the digital logic circuit applications, the study (Sniatała et al., 2007) applied Xilinx CPLD XC9572 based commercial board to test a new structure of an integrator. The paper (Petrescu et al., 2015) utilized Digilent Basys2 commercial board as a demonstration tool for the laboratory works. The reference (Chinedu et al., 2011) applied Cypress CY37256P160 based commercial peripheral board to design a liquid dispenser controller system. However, the study (Slee et al., 2009) have introduced the causes of the printed circuit board (PCB) failures, including burning propagating faults, bad connection issues, component failures of age factors and overheating environmental

problems. Therefore, it is necessary to develop the circuit board tester for the PCB specifically. The thesis (Wu, 2014) implemented 3 examination questions in the CPLD single chip for testing the PCB of digital electronics technician authentication. The study (Lin, 2008) proposed a wireless testing system to decrease the bit error rate by using embedded built-in self-test FPGA/CPLD device with RF module. The literature (Houdek, 2016) overviewed the inspection and testing methods for PCBs and suggested the key techniques, such as visual, physical and IC test, used to troubleshoot a circuit board. The research (Serban et al., 2014) proposed a test platform at the functional level. In contrast to existing troubleshooting techniques designed only for testing one particular PCB, the proposed platform is universal and can be easily reconfigured and reprogrammed to test different PCBs. Two articles have also proposed circuit board functional test technology. The study (Lotz et al., 2006) analyzed the functional board test strategy to validate the design and detect structural defects during the production. The study (Elssamadisy and Whitmor, 2006) stated the advantages of the functional test, such as enabling elucidating project requirements, making project progress visible, preventing bugs and increasing business values.

With the rapid development of the integrated circuit design, system-on-chip (SoC) designs with specific functions have become more diversity. Therefore, designing the SoC coupled with complex functions makes testing more difficult than before. In general, designing, compiling, and downloading a specific functional-based module of Built-In-Circuit-Test (BICT) into the CPLD chip can be used to troubleshoot the CPLD device and test the circuit board. However, in the scenario of testing diverse peripheral devices, re-designing and re-compiling the circuits are necessary for testing different peripheral devices. Therefore, this paper extends the author's previous research (Chao and Hsu, 2019) to develop an educational tool which integrates multifunctional circuits into the EPM 7064SLC44-10 CPLD based commercial circuit board. In order to ensure that the PCB used in the course can work functional correctly, the proposed approach allows users capturing the input signals and transmitting the outputs to peripheral devices after the designed multifunctional circuits downloaded into the CPLD chip. In addition, the designed integrated circuits can be easily reconfigured and reprogrammed to test different CPLD chips or PCB circuit boards. The proposed educational tool can also help the beginners quickly learning the use of the experimental instruments, easily understanding the practical training contents, and accurately finishing every experiment.

2. Material and Methods

This paper proposes a circuit board functional test technique which utilizes the integrating technology of the multifunctional digital logic circuits to detect whether the input and output devices on the circuit board can work correctly. The input devices of the circuit board include clocks, dip switches and push buttons; the output devices of the circuit board include the buzzer, LEDs and 7-segment displays. The proposed approach mainly integrates four digital logic circuits into the CPLD integrated chip (IC) for troubleshooting the circuit board in advance as well as increasing the learning effects on integrated circuit design skills. Three designing processes, including integrating four digital logic circuits, adding enabling control signal to every original digital logic circuit, and planning the integrated circuits into the chip, are described as follows respectively.

2.1. Integrating Four Digital Logic Circuits

Figure 1 illustrates the structure of the circuit board functional tester in which a 2X4 decoder is used to control four different digital logical circuit designs. As shown in Figure 1, four different digital logic circuits include 7-segment display control, 1X4 de-multiplexer, 4X2 coder, and 6-dice random display. Table 1 presents the truth table of integrating four digital logic circuits. As shown in Table 1, when the input is in the condition of "BA=00", 7-segment display control circuit is enabled by the "E1" control signal. When the input in the condition of "BA=01", 1X4 de-multiplexer circuit is enabled by the "E2" control signal. When the input is in the condition of "BA=10", 4X2 coder circuit is enabled by the "E3" control signal. When the input is in the condition of "BA=11", 6-dice random display circuit is enabled by the "E4" control signal.

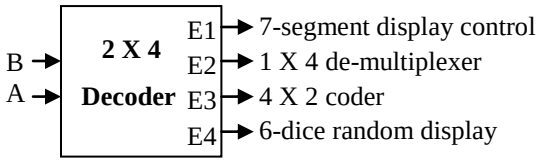


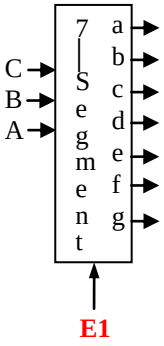
Figure 1. Structure of the circuit board functional tester.

Table 1. Truth table of four digital logic circuits

Inputs B A	Output Y	Functions
0 0	E1	7-segment display control
0 1	E2	1 X 4 de-multiplexer
1 0	E3	4 X 2 coder
1 1	E4	6-dice random display

2.2. Adding Enabling Control Signal to Every Original Digital Logic Circuit

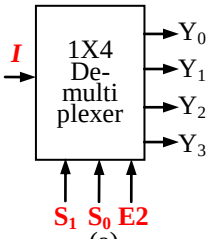
Figure 2 presents the input/output structures of 7-segment display control circuit with the enabling signal as well as its corresponding truth table. Figure 3 presents the input/output structures of 1X4 de-multiplexer circuit with the enabling signal as well as its corresponding truth table. Figure 4 presents the input/output structures of 4X2 coder circuit with the enabling signal as well as its corresponding truth table. Figure 5 presents the input/output structures of 6-dice random display circuit with the enabling signal as well as its corresponding truth table. As shown in Figure 5, when the input clock switch is pressed, the dice randomly displays different points and the buzzer rings at the same time.



E1	Inputs C B A	Outputs a b c d e f g	
0	0 0 0	0 0 0 0 0 0 1	0
0	0 0 1	1 0 0 1 1 1 1	1
0	0 1 0	0 0 1 0 0 1 0	2
0	0 1 1	0 0 0 0 1 1 0	3
0	1 0 0	1 0 0 1 1 0 0	4
0	1 0 1	0 1 0 0 1 0 0	5
0	1 1 0	0 1 0 0 0 0 0	6
0	1 1 1	0 0 0 1 1 1 1	7

(a) (b)

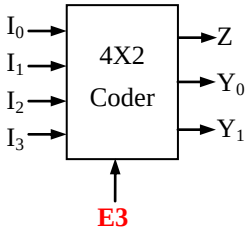
Figure 2. (a)Input/output structures of 7-segment display with the enabling signal; (b) input/output truth table.



E2	Input *I* & Selection S_1 S_0	Outputs Y_3 Y_2 Y_1 Y_0
0	0 0	1 1 1 *I*
0	0 1	1 1 *I* 1
0	1 0	1 *I* 1 1
0	1 1	*I* 1 1 1

(a) (b)

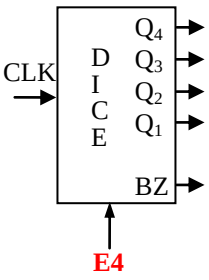
Figure 3. (a)Input/output structures of 1X4 de-multiplexer with the enabling signal; (b) input/output truth table.



E3	Inputs I_3 I_2 I_1 I_0	Outputs Z Y_0 Y_1
0	X X X 1	1 0 0
0	X X 1 0	1 0 1
0	X 1 0 0	1 1 0
0	1 0 0 0	1 1 1
0	0 0 0 0	0 1 1

(a) (b)

Figure 4. (a) Input/output structures of 4X2 coder with the enabling signal; (b) input/output truth table.



E4	Input CLK	Outputs Q_4 Q_3 Q_2 Q_1	
0	1	1 0 1 1	
0	2	1 1 1 0	
0	3	1 0 1 0	
0	4	1 1 0 0	
0	5	1 0 0 0	
0	6	0 1 0 0	

(a) (b)

Figure 5. (a) Input/output structures of 6-dice random display with the enabling signal; (b) input/output truth table.

2.3. Planning the Integrated Circuits into the Chip

Figure 6 shows the 44-pin CPLD EPM 7064SLC44-10 chip of MAX7000S family. Figure 7 illustrates the pin allocations of the integrated circuits. As shown in Figure 7(a), the 8-LED output pin allocations are used for displaying the output states of 1X4 de-multiplexer, 4X2 coder and 7-segment designed circuits. As for the Figure 7(b), the buzzer and LED output pin allocations are used for enabling buzzer sound and displaying the output states of 6-dice designed circuit. In addition, the input pin allocations contain three parts. As shown in Figure 7(c), the input DIP-8 pin allocations are used for the input DIP switches of 1X4 de-multiplexer, 4X2 coder and 7-segment designed circuits. As for Figure 7(d), the input clock push-button pin is used for triggering 6-dice designed circuit; the 4 push-button selection pins are used for controlling and enabling four different digital logical designed circuits.

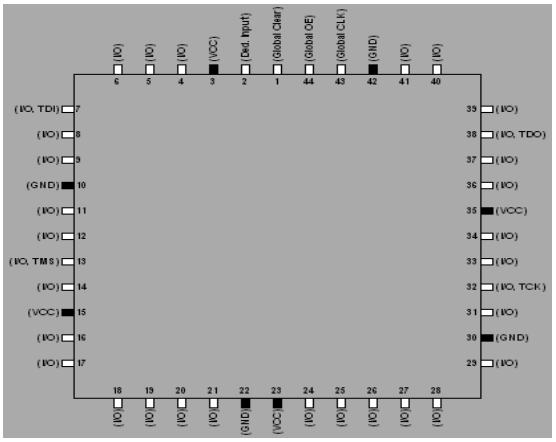


Figure 6. 44-pin CPLD EPM 7064SLC44-10 chip of MAX7000S family.

8-LED Output Indicators							
P21	P24	P25	P26	P27	P28	P29	P31

(a)

Buzzer	6-Dice Output Indicators			
P20	P36	P37	P39	P40

(b)

Input DIP-8 Switch Pins							
P04	P05	P06	P08	P09	P11	P12	P14

(c)

Input Clock Pin	Input Selection Pins				
Push-Buttons	P43	P16	P17	P18	P19

(d)

Figure 7. Pin allocations; (a) 8-LED output indicators; (b) buzzer and 6-dice output indicators; (c) input DIP-8 switch pins, (d) input clock and input selection pins.

3. Results

In this paper, the author adopts the CPLD EPM 7064SLC44-10 based commercial circuit board and Altera Quartus II software as the experimental tools. Figure 8 illustrates the schematics of integrated four different digital logic circuits, including 7-segment, 1X4 de-multiplexer, 4X2 coder and 6-dice. Figure 9 shows the picture of the EPM 7064SLC44-10 based commercial peripheral board which is developed by Taiwan Embedded Microcontroller Development Institution (TEMI). A user can find the detail circuit schematics and related references from the website of TEMI. As shown in Figure 9, the peripheral board supports several functions, such as multi-clock input selections, functional setting input DIP switches, input DIP switches, input pushbuttons, LED outputs, 7-segment outputs, dice outputs, and buzzer output. In addition, the pin allocations of S3 and S4 push buttons are assigned and the designed circuits can be downloaded into the chip either by parallel port or USB port. Figure 10 demonstrates the pin allocations and functional verification of 7-segment logical circuit design. Figure 11 and Figure 12 present the pin allocations and functional verifications of 1X4 de-multiplexer and 4X2 coder combinational logical circuit designs, respectively. Figure 13 shows 6-dice random display with buzzer sound of the sequential logical circuit design. In addition, there are extra educational resources for users, including the functional verification procedures and the operational manual of the designed circuits as well as providing troubleshooting methods for the circuit board functional test.

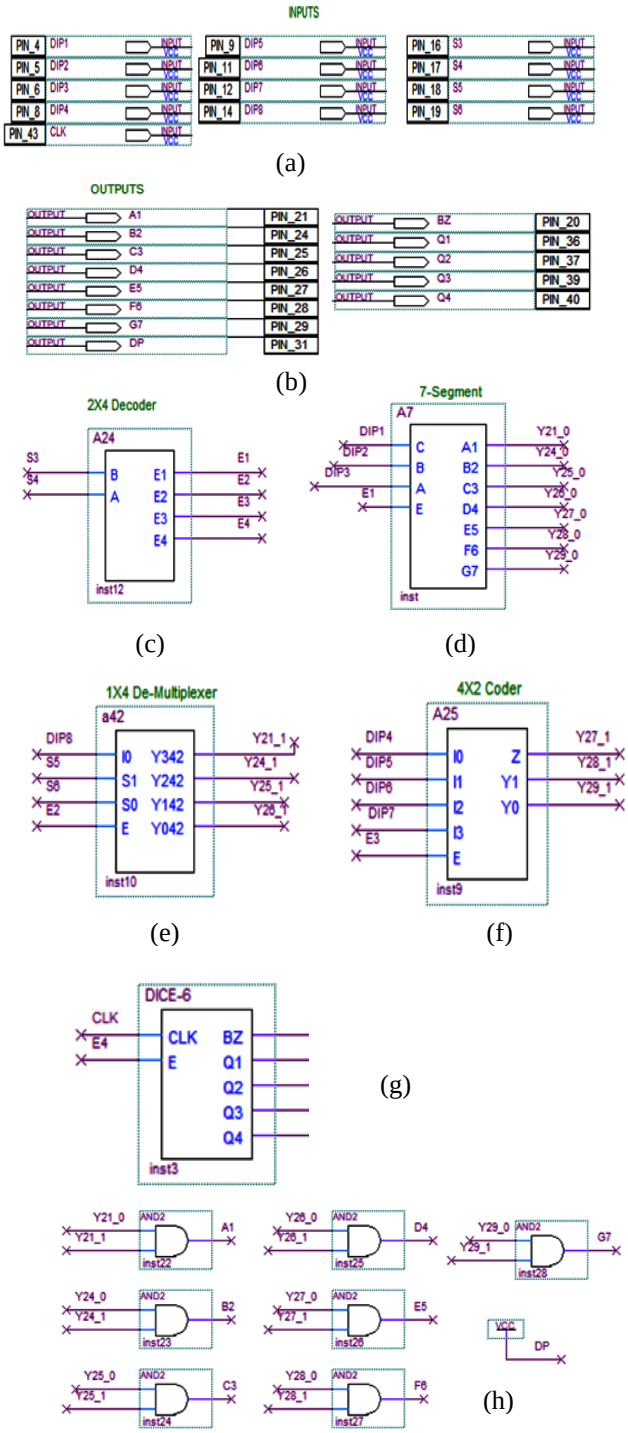


Figure 8. Schematics; (a) inputs pin assignments; (b) outputs pin assignments; (c) 2X4 decoder; (d) 7-Segment display; (e) 1X4 de-multiplexer; (f) 4X2 coder; (g) 6-dice random display; (h) logic circuitries for sharing the outputs.

3.1. Pin Allocation of 2X4 Decoder

(1) Inputs: S3(pin16), S4(pin17)
(2) Outputs: E1, E2, E3, E4

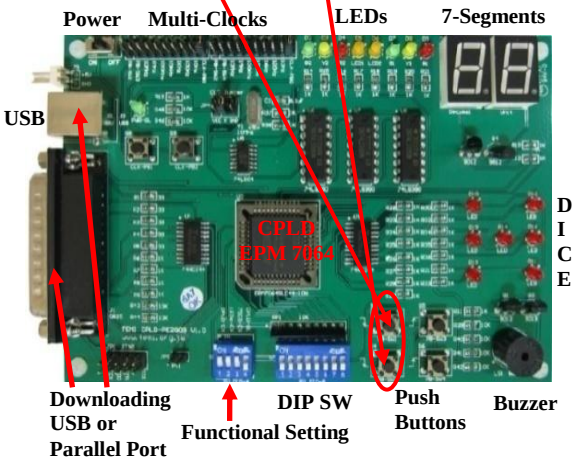


Figure 9. CPLD EPM 7064SLC44-10 based peripheral board.

0: Press the push button; 1: No action.

Inputs S3 S4	Output Y
0 0	E1
0 1	E2
1 0	E3
1 1	E4

3.2. Pin Allocations of 7-Segment Displays

(1) Inputs: S3(pin16), S4(pin17), C (pin 4) , B(pin5), A(pin6)
(2) Control Pin: E1
(3) Outputs: A1(pin21), B1(pin24), C1(pin 25), D1(pin26), E1(pin27), F1(pin28), G1(pin29)

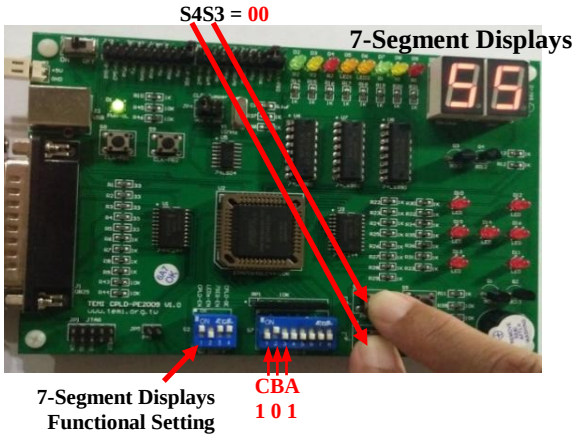


Figure 10. 7-segment displays pin allocations and functional verification.

3.3. Pin Allocation of 1X4 De-Multiplexer

(1) Inputs: *I* (pin 14), S3(pin16), S4(pin17), S5(pin 18), and S6(pin19)
(2) Control Pin: E2
(3) Outputs:Y3(pin21), Y2(pin24), Y1(pin25), Y0(pin26)

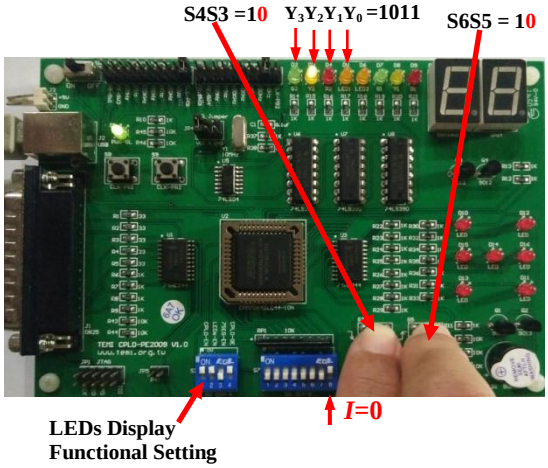


Figure 11. 1X4 de-multiplexer pin allocations and functional verification.

3.4. Pin Allocation of 4X2 Coder

(1) Inputs: S3(pin16), S4(pin17), I_0 (pin 8) , I_1(pin9), I_2(pin11), and I_3(pin12)
(2) Control Pin: E3
(3) Outputs: Z(pin27), Y1(pin21), Y0(pin21)

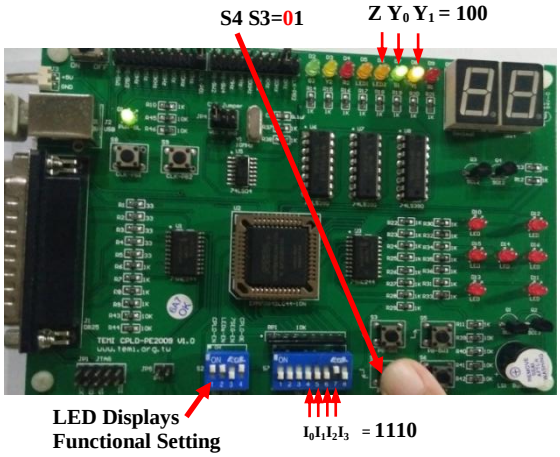


Figure 12. 4X2 coder pin allocations and functional verification.

3.5. Pin Allocation of 6-Dice Random Display

(1) Inputs: S3(pin16), S4(pin17), CLK-PB1 (pin 43) with 10Hz
(2) Control Pin: E4
(3) Outputs: BZ(pin20), Q3(pin40), Q2(pin39), Q1(pin37) and Q0(pin36)

When the CLK-PB1 control button is pressed, the buzzer will sound and the dice display will repeat the number of 1 -> 2 -> 3 -> 4 -> 5 -> 6 -> 1- > 2 ... points until the CLK-PB1 button is released.

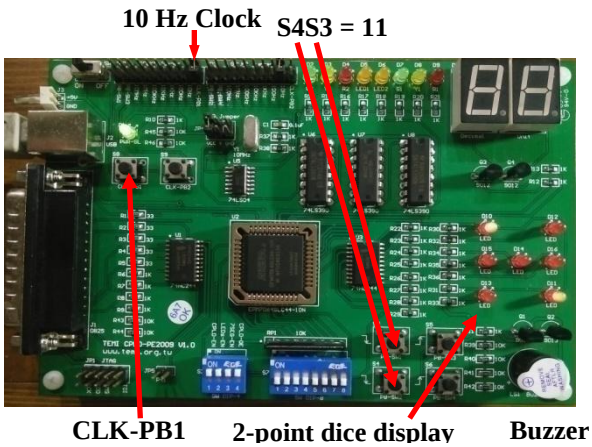


Figure13. 6-dice random display with buzzer sound pin allocations and functional verification.

4. Conclusions

In order to enhance the teaching quality and increase the learning effects, this paper proposes a hardware troubleshooting technique for testing the function of the EMP7064SLC44-10 based CPLD circuit board, which can be used at the beginning of the practical training course for demonstrating the multifunctional IC design skills. The proposed circuit board tester provides three advantages. First, the designed functional-based module of Built-In-Circuit-Test (BICT) CPLD chip can test the CPLD device and different peripheral devices on the circuit board without re-designing and re-compiling the circuits. Second, the designed integrated circuits can provide students not only to learn the essential contents of digital logic circuit design skills but also to understand the method of designing a system-on-chip (SoC) with specific functions. Third, the proposed testing technology can help the beginners easily learn the use of the experimental instruments, quickly understand the practical training contents, and accurately finish every experiment as well as can attract more students interesting in planning, designing and implementing IC design related projects.

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