An Effective Teaching Tool for Digital Logic Circuit Design

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Abstract: An effective teaching tool used for learning digital logic circuit design is proposed in this paper. The proposed teaching tool mainly integrates the examination questions of the capability certification, including five specific combinational and sequential digital logic circuits, into EMP7064SLC44-10 Complex Programmable Logic Device (CPLD) single chip. Five specific combinational digital circuits are the adder/subtractor, coder, decoder, multiplexer and de-multiplexer. Five distinctive sequential digital circuits are the ripple counter, synchronized counter, up/down counter, and loop counter. The designed integrated circuit (IC) chip with multifunctional digital logic circuits is experimented by using Altera MAX+Plus II software for circuitry designing, compiling, simulating, floor-planning, and programming processes. According to the experimental results, the proposed teaching tool can increase the teaching quality and learning effects by demonstrating multifunctional IC design skills as well as can increase the passing rate of the practical level capability certification for digital logic circuit design.
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1. Introduction

Over the past decade, with the integrated circuit (IC) design industry boomed and the advanced complex programmable logic device (CPLD) technology developed, applying system on chip (SOC) and CPLD technology in the application-specific integrated circuit (ASIC) design is with a high demand for specific customized product development. In the reviewing some references applying the CPLD to develop the specific customized product, the study (Tsai and Chen, 2002) designed a decoder/counter interface IC for motor control. The paper (Ali and Kshirsagar, 2010) developed an open loop stepper motor controller. The reference (Samman and Syarnsuddin, 2002) introduced the programmable fuzzy logic controller. The literature (Tsai et al., 2004) designed a digital programmable control IC for common-neutral half-bridge bilateral AC-DC-AC Converters. In the reviewing some references related to applying CPLD based commercial peripheral boards in the digital logic circuit applications, the study (Sniatała et al., 2007) applied Xilinx CPLD XC9572 based commercial board to test a new structure of an integrator. The paper (Petrescu et al., 2015) utilized Digilent Basys2 commercial board as a demonstration tool for the laboratory works. The reference (Chinedu et al., 2011) applied Cypress CY37256P160 based commercial peripheral board to design a liquid dispenser controller system.

Generally, digital logic circuit design in colleges is an important and fundamental subject for students majoring in Electrical/Electronic/Mechanical Engineering because it is the basis of developing the mechanical/electrical controls, embedding system designs, and microcontroller related applications. At Electronic Engineering department of Kao Yuan University in Taiwan, the digital logic circuit design courses have been scheduled for two-semester courses. One semester is a requirement for junior students and the other one semester is an elective for senior students. In order to achieve effective teaching quality in an institute, a teacher generally needs to know how the students can learn well. The literature (Abedi and Badragheh, 2011) stated that adult education needs to account for motivation of the learner, reinforcement of the skill, retention of key learning, and transference of what is learn of new situations. The authors (Badragheh and Abedi, 2011) also suggested that the ways to strengthen adult education are such as offering a variety of formats, schedules, and approaches, meeting people where they are, promoting participation effectively, and fostering strong leadership. In addition, there are some references adopting hardware description languages, including VHDL, AHDL, and IEEE-1076 industrial standard language, for CPLD/FPGA programmable logic devices in the logic design course. The study (Areibi, 2001) integrated VHDL and programmable logic devices with Quartus II software tool into the logic design course. The paper (Chang, 1996) introduced the top-down design methodology through VHDL compiler, logic synthesizer, functional and timing simulator, floor plan editor and programmer to learn how to partition a complex design into small

components in the senior digital logic design course. The literatures (Sugita, 1994; Rais et al., 2012) introduced different CPLD characteristics of Altera MAX 7000 family, which could be used as a reference for developing different CPLD based applications.

In the considering of related digital logic circuit design capability certification, Taiwan Embedded System Development Association (TEMI) has issued the practical and professional levels of the capability certifications for digital logic circuit design Obtaining such capability certification helps users to demonstrate their professional capabilities of the digital logic integrated circuit design and peripheral interface control skills. A user is qualified for obtaining the practical certificate only if he/she can pass the test on both combinational and sequential logical circuit design by using EPM 7064SLC44-10 CPLD chip. As for the professional certificate, a user has to pass the examinations of both software and hardware digital logic application design. Therefore, based on the teaching principles described above, this paper extends the authors' previous research (Chao and Hsu, 2016) to develop an effective teaching tool used for learning digital logic circuit design. The study applies EPM 7064SLC44-10 CPLD based commercial peripheral board coupled with MAX+ Plus II software for testing the designed circuits. In addition, the authors integrates the examination questions of the capability certification into the CPLD single chip to help users learning contents of the examination questions quickly, increasing the learning effects on integrated circuit design, and raising the passing rate of the practical level capability certification for digital logic circuit design.

2. Material and Methods

Figure 1 illustrates the structure of the digital logic circuit design teaching tool in which a 4X16 decoder is used to control different digital logical circuit designs. Table 1 gives the truth table of integrating five combinational and five sequential examination questions of the capability certification for the digital logic circuit design. As shown in Table 1, when the input "E=0", the system chip is enabled into the combinational digital logic circuit design mode in which input "CBA=000" controls the half adder/subtractor circuit design, input "CBA=001" and "CBA=010" control the coder/decoder circuit designs, input "CBA=011" and "CBA=100" control the multiplexer/de-multiplexer circuit designs. For the condition of the input "E=1", the system chip is enabled into the sequential digital logic circuit design mode in which input "CBA=000" controls module-8 ripple counter circuit design, input "CBA=001" and "CBA=010" control synchronized module-6 up counter and module-5 down counter circuit design, input "CBA=011" and "CBA=100" control module-4 loop counter and module-7 Johnson counter circuit design. The following describes their detail functions and design methodologies.

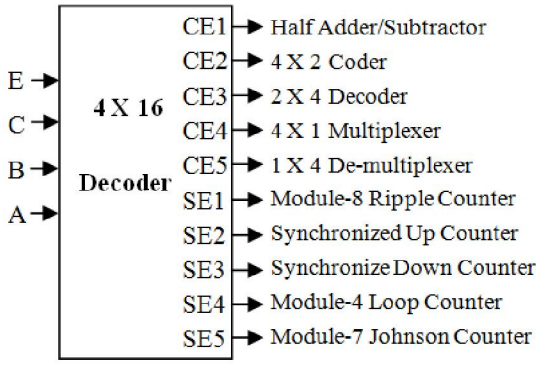


Figure 1. Structure of digital logic circuit design.

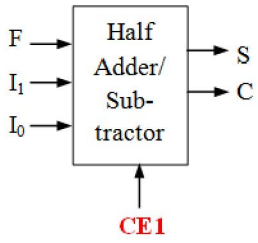
Table 1. Truth table of integrating five different combinational/sequential examination questions.

Inputs				Output
E	C	B	A	Y
0	0	0	0	Half Adder/Subtractor
0	0	0	1	4 X 2 Coder
0	0	1	0	2 X 4 Decoder
0	0	1	1	4 X 1 Multiplexer
0	1	0	0	1 X 4 De-multiplexer
1	0	0	0	Module-8 Ripple Counter
1	0	0	1	Synchronized Up Counter
1	0	1	0	Synchronize Down Counter
1	0	1	1	Module-4 Loop Counter
1	1	0	0	Module-7 Johnson Counter

2.1. Combinational digital logic circuit design

Five combinational digital logic circuits including 2-bit half adder/subtractor, 4X2 coder, 2X4 decoder, 4X1 multiplexer, and 1X4 de-multiplexer of the practical certification questions are introduced in this section. Figure 2 presents the input/output structures of 2-bit half adder/subtractor with enabling signal as well as its corresponding truth table. As shown in Figure 2, when "CE1=0", the circuit of the half adder/subtractor is enabled. Figure 3 presents the input/output structures of 4X2 coder with enabling signal as well as its corresponding truth table. As shown in Figure 3, when "CE2=0", the circuit of the 4X2 coder is enabled. Figure 4 presents the input/output structures of the 2X4 decoder with enabling signal CE3 marked in red color. As shown in Figure 4, when "CE3=0", the circuit of the 2X4 decoder is enabled. Figure 5 presents the input/output structures of the 4X1 multiplexer with enabling signal CE4 marked in red color. As shown in Figure 5, when

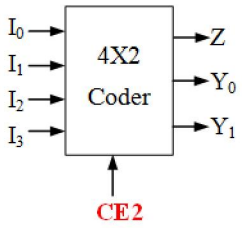
"CE4=0", the circuit of the 4X1 multiplexer is enabled. Figure 6 shows the input/output structures of the 1X4 de-multiplexer with enabling signal CE5 marked in red color. As shown in Figure 6, when "CE5=0", the circuit of the 1X4 de-multiplexer is enabled.



CE1	Inputs F	I_1	I_0	Outputs S	C
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	1	0
0	0	1	1	0	0

(a) (b)

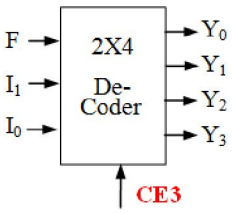
Figure 2. (a) Input/output structures of half adder/ subtractor with enabling signal; (b) input/output truth table.



CE2	Inputs I_3	I_2	I_1	I_0	Outputs Z	Y_0	Y_1
0	X	X	X	1	1	0	0
0	X	X	1	0	1	0	1
0	X	1	0	0	1	1	0
0	1	0	0	0	1	1	1
0	0	0	0	0	0	1	1

(a) (b)

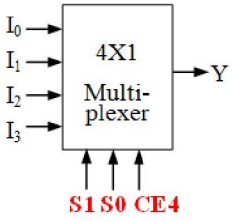
Figure 3. (a) Input/output structures of 4X2 coder with enabling signal; (b) input/output truth table.



CE3	Inputs F	I_1	I_0	Outputs Y_3	Y_2	Y_1	Y_0
0	0	X	X	1	1	1	1
0	1	0	0	1	1	1	0
0	1	0	1	1	1	0	1
0	1	1	0	1	0	1	1
0	1	1	1	0	1	1	1

(a) (b)

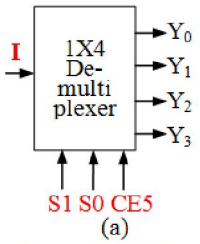
Figure 4. (a) Input/output structures of 2X4 decoder with enabling signal; (b) input/output truth table.



CE4	Inputs	Selections S_1	S_0	Output Y
0		0	0	I_3
0	I_0 I_1	0	1	I_2
0		1	0	I_1
0	I_2 I_3	1	1	I_0

(a) (b)

Figure 5. (a) Input/output structures of 4X1 multiplexer with enabling signal; (b) input/output truth table.



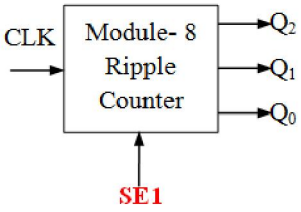
CE5	Input *I* & Selection S_1	S_0	Outputs Y_3	Y_2	Y_1	Y_0
0	0	0	1	1	1	*I*
0	0	1	1	1	I	1
0	1	0	1	*I*	1	1
0	1	1	I	1	1	1

(a) (b)

Figure 6. (a) Input/output structures of 1X4 Demulti-plexer with enabling signal; (b) input/output truth table.

2.2. Sequential Digital Logic Circuit Design

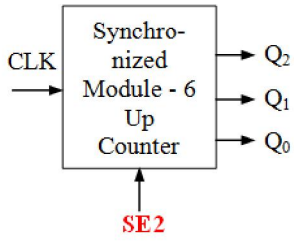
Five sequential digital logic circuits including module-8 ripple counter, synchronized module-6 up counter, module-5 down counter, module-4 loop counter, and module-7 Johnson Counter of the practical certification questions are introduced in this section. Figure 7 presents the input/output structures of the module-8 ripple counter with enabling signal as well as its corresponding truth table. As shown in Figure 7, when "SE1=0", the circuit of the module-8 ripple counter is enabled. Figure 8 presents the input/output structures of the synchronized module-6 up counter with enabling signal as well as its corresponding truth table. As shown in Figure 8, when "SE2=0", the circuit of the synchronized module-6 up counter is enabled. Figure 9 presents the input/output structures of the synchronized module-5 down counter with enabling signal SE3 marked in red color. As shown in Figure 9, when "SE3=0", the circuit of the synchronized module-5 down counter is enabled. Figure 10 presents the input/output structures of the module-4 loop counter with enabling signal SE4 marked in red color. As shown in Figure 10, when "SE4=0", the circuit of the module-4 loop counter is enabled. Figure 11 shows the input/output structures of the module-7 Johnson Counter with enabling signal SE5 marked in red color. As shown in Figure 11, when "SE5=0", the circuit of the module-7 Johnson Counter is enabled.



SE1	Input CLK	Outputs Q_2	Q_1	Q_0
0	0	1	1	1
0	1	1	1	0
0	2	1	0	1
0	3	1	0	0
0	4	0	1	1
0	5	0	1	0
0	6	0	0	1
0	7	0	0	0
0	8	1	1	1

(a) (b)

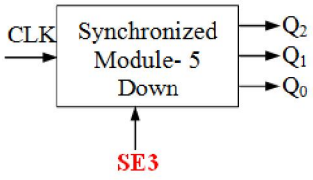
Figure 7. (a) Structures of module-8 ripple counter with enabling signal; (b) input/output truth table.



SE2	Input CLK	Outputs Q2 Q1 Q0
0	0	0 0 0
0	1	0 0 1
0	2	0 1 0
0	3	0 1 1
0	4	1 0 0
0	5	1 0 1
0	6	0 0 0

(a) (b)

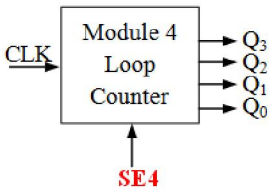
Figure 8. (a) Structures of synchronized module-6 up counter with enabling signal; (b) input/output truth table.



SE3	Input CLK	Outputs Q2 Q1 Q0
0	0	1 0 0
0	1	0 1 1
0	2	0 1 0
0	3	0 0 1
0	4	0 0 0
0	5	1 0 0

(a) (b)

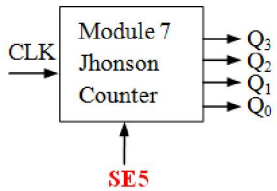
Figure 9. (a) Structures of synchronized module-5 down counter with enabling signal; (b) input/output truth table.



SE4	Start	Input CLK	Outputs Q3 Q2 Q1 Q0
0	0	0	0 0 0 1
0	1	1	0 0 1 0
0	1	2	0 1 0 0
0	1	3	1 0 0 0
0	1	4	0 0 0 1

(a) (b)

Figure 10. (a) Structures of synchronized module-4 loop counter with enabling signal; (b) input/output truth table.



SE5	Input CLK	Outputs Q3 Q2 Q1 Q0
0	0	0 0 0 0
0	1	0 0 0 1
0	2	0 0 1 1
0	3	0 1 1 1
0	4	1 1 1 0
0	5	1 1 0 0
0	6	1 0 0 0
0	7	0 0 0 0

(a) (b)

Figure 11. (a) Structures of synchronized module 7 Johnson counter with enabling signal; (b) input/ output truth table.

2.3. Planning the Integrated Circuits on a Chip

Figure 12 shows the 44-pin CPLD EPM 7064SLC44-10 chip of MAX7000S family. Figure 13 illustrates the pin allocations of the integrated circuits. As shown in Figure 13(a), the output pin allocations are used for displaying each digital logic circuit output states. As for the Figure 13(b), the output pin allocations are used for indicating either the combinational or the sequential circuits is enabled. There are three parts for the input pin allocations. As shown in Figure 13(c), the input pin allocations apply 4 pins of DIP switches as the inputs for digital logic circuits and the other 4 pins of DIP switches are used as the enabling control for different digital logical circuit designs. As for Figure 13(d) and (e), the input pins of clear, clock and selection switches are assigned to the pin 13, 43, 16, and 17 respectively.

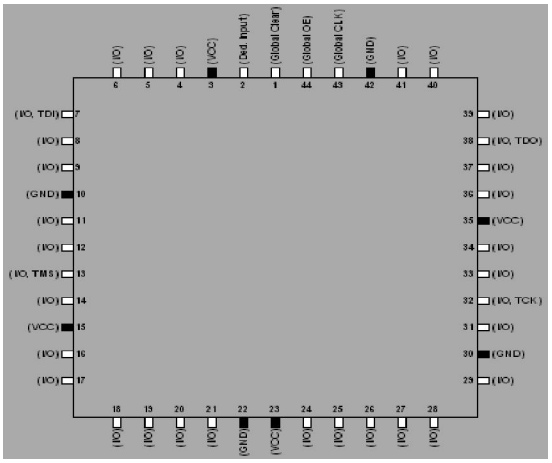


Figure 12. 44-pin diagram of CPLD EPM 7064SLC44-10 chip.

8 LED Outputs							
P21	P24	P25	P26	P27	P28	P29	P31

(a)

Output Indicators for Enabling Questions of Combinational/Sequential Circuits					
P33	P34	P36	P37	P39	P40

(b)

Input DIP-8 Switch Pins							
P04	P05	P06	P08	P09	P11	P12	P14

(c)

Input Clear and Clock pins	
P13	P43

(d)

Input Selection Pins	
P16	P17

(e)

Figure 13. Pin allocations; (a) 8 LED outputs; (b) output indicators; (c) input DIP-8 switches, (d) input clear and clock pins; (e) input selection pins.

2.3.1 Functional Demonstration of 4X1 Multiplexer

(1) Input: I_0 (pin 4), I_1(pin5), I_2(pin6), and I_3(pin8), S0(pin 16), and S1(pin17)

(2) Outputs: Y (pin21)

(3) Control Pins: E (pin 9), C (pin 11), B (pin 12), A (pin 14)

(4) Output Indicators:

Combinational/Sequential Circuit: Pin 33 and Pin 34

Number of the questions: Pin 36, 37, 39, and Pin 40.

2.3.2 Functional Demonstration of Module-8 Ripple Counter

(1) Input: Clock (pin 43) with 10Hz

(2) Outputs: Q_2(pin21), Q_1(pin24) and Q_0(pin25)

(3) Control Pins: E (pin 9), C (pin 11), B (pin 12), A (pin 14)

(4) Output Indicators:

Combinational/Sequential Circuit: Pin 33 and Pin 34

Number of the questions: Pin 36, 37, 39, and Pin 40.

3. Results

In this paper, the authors adopt the EPM 7064SLC44-10 CPLD based commercial peripheral board and Altera MAX+Plus II software as the experimental tools to integrate both combinational and sequential digital logic circuits into one chip. Figure 14 shows the picture of the EPM 7064SLC44-10 based commercial peripheral board which is developed by Taiwan Embedded Microcontroller Development Institution (TEMI). A user can find the detail circuitry schematics (Chao, 2013) and related references at the website of TEMI. As shown in Figure 14, the peripheral board supports several functions, including selecting multi-clock inputs, four specific DIP switches for functional setting, 8-pin DIP switches for inputs, 4 pushbuttons for inputs, 8 LEDs for outputs, two 7-segment displays for outputs, 7 dices for outputs, and the buzzer for the sound output. In addition, this peripheral board allows users down loading the designed circuit in to the chip either by parallel port or USB port.

Figure 15 demonstrates the pin allocations and functional verification of the 4X1 multiplexer, which is the fourth question of the combinational logical circuit design. As shown in Figure 15, when "S1S0=11" and "ECBA=0100", the input "I_0=0" state is shown on the output "Y=0". Figure 16 presents the pin allocations and functional verification of the module-8 ripple counter, which is the first question of the sequential logical circuit design.

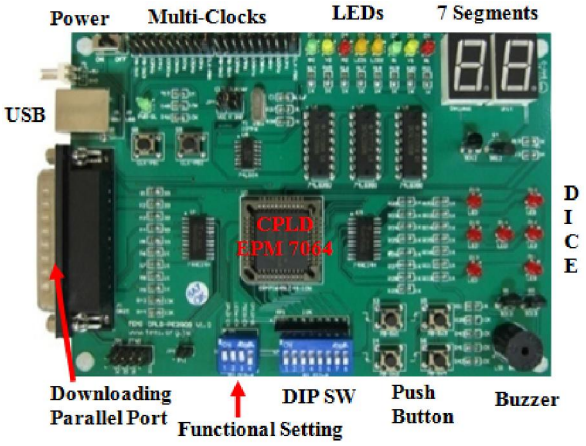


Figure 14. CPLD EPM 7064SLC44-10 based peripheral board.

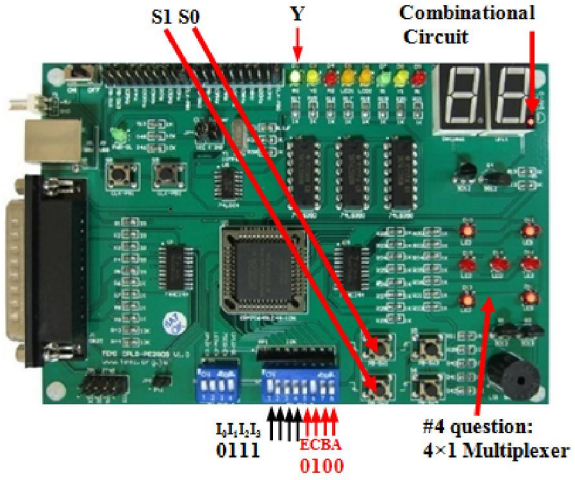


Figure 15. 4X1 multiplexer pin allocations and functional verification.

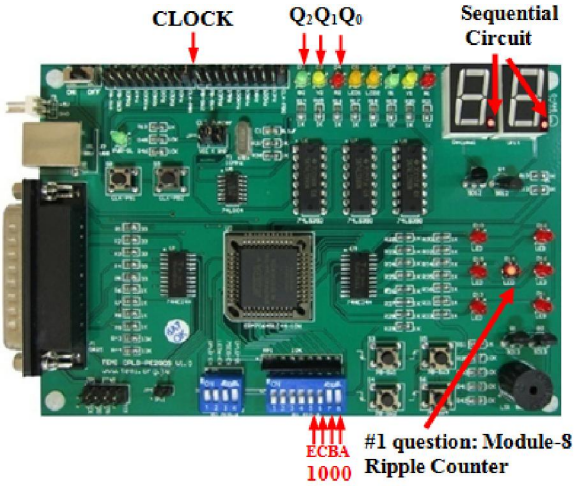


Figure 16. Module-8 ripple counter pin allocations and functional verification.

4. Conclusions

This study mainly integrates the examination questions of the capability certification, including five specific combinational and sequential digital logic circuits, into EPM 7064SLC44-10 CPLD single chip. The goal is to help students understanding the contents of the capability certification, learning the integration of multifunctional circuit design skills, and increasing the passing rate of the practical level capability certification for digital logic circuit design. The proposed teaching tool is different from the traditional digital logic circuit design course in three aspects. First, students not only learn the essential contents of the digital logic circuit design skills but also know the project oriented design method for the integrated circuit (IC) technology. Second, the use of the commercial peripheral board with diversity input and output interfaces can provide students with brainstorm training on specific IC design technology effectively and efficiently. Third, the constructed teaching tool can attract more students interesting in planning, designing and implementing solutions to the project as well as cultivating more qualified digital logic integrated circuit design engineers for local industries.

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