Statistical Analysis Based Signature Extraction Methodology for Fault Detection of Power Electronic Circuits

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Abstract: In this paper, statistical analysis is made use of to develop a fault dictionary. A three phase single level Voltage Source Inverter (VSI) circuit is being chosen as Circuit Under Test (CUT). The output of the CUT is subjected to wavelet transform. Based on the transform coefficients for the fault free circuit as well as simulated faults for the CUT, fault dictionary has been framed. Fault dictionary is being generated by extracting the standard deviation (from statistical analysis) of the transform coefficients. Extracted parameters are utilized to develop the fault dictionary, which is later used for fault identification. The method has been validated using a single phase multilevel inverter circuit.
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Keywords: Fault detection; Statistical analysis; Wavelet Transform; Three Phase Single Level VSI; Single Phase Multilevel Inverter; Fault Dictionary

1. Introduction

Fault diagnosis is an inevitable measure in ensuring the competent performance of the circuit. Hence analog testing plays a key role in the circuit industry. The prime goal of the industry is to maintain stability of the circuit. This becomes a tedious task owing to its complexity. To ensure reliability and safety of any system under study, Fault Detection and Isolation (FDI) is highly required.

A circuit which behaves in an unexpected manner is said to be a faulty circuit. Catastrophic and parametric faults are the two kinds of failure modes of analog circuits. A set of catastrophic faults may be derived from its layout for analog IC while parametric faults are difficult to build.

Fault diagnosis approaches are of many types namely fault dictionary approach, the parameter identification approach, the fault verification approach, the approximation approach, the artificial intelligence technique and so on (Rozailan et al., 2006), (Rothenhagen and Fuchs, 2005), (Renfrew and Tian, 1993), (Bandler and Salama, 1985), and (Tadeusiewicz et al., 2002). In general the fault diagnosis approaches of analog circuit can be categorized into two namely, Simulation-Before-Test (SBT) and Simulation-After-Test (SAT). SAT involves the computation of various parameters that are required to build in the fault dictionary. These parameters are being extracted from the operational circuit. Assuming that the each parameter is independent of the other, fault identification is being carried out. But when the size of the circuits is increased the processing time is also increased. Hence this method is usually avoided. While in SBT approach (Dubois and Prade, 1980), (Abramic et al., 2003), (Mckeon and Wakeling, 1989), and (Gertler, 1998) the signatures are extracted by simulating a finite set of arbitrary test conditions that are unique to each faulty condition and it appreciably reduces the time taken for fault diagnosis. These signatures can be suitably used to create a fault dictionary, a collection of measurement of a network under different potential faults. The condition for avoiding masking of any faults is that the parameters chosen for signatures must be observable for all conditions of the circuit.

Intuitional knowledge of the functioning of the CUT is not required as both the approaches are procedural in nature. Fault detection and isolation altogether marks fault diagnosis. Early detection of fault can possibly avoid the damages borne out of the fault and can ensure safety and reliability of the circuit.

The most prominent sources of fault in a power electronic circuit are the semiconductor switches. The faults in these switches can be either short circuit faults or open circuit faults. The occurrence of open circuit fault is very rare. But the open circuit fault may create overstress on other components leading to its failure. Hence its inclusion

in the fault diagnostic procedure has become mandatory.

The voltage source inverter is chosen as the CUT. A three phase single level IGBT based VSI was modeled using MATLAB. Its each phase was analyzed using wavelet transform.

2. Wavelet Theory

The Wavelet means a 'small wave'. Its nomenclature as a wave can be attributed to its oscillatory nature. The wavelet analysis involves analyzing a signal with short duration finite energy functions. Thus the signal under investigation is being transformed into another representation of more useful format.

This signal transformation is called Wavelet Transform. Wavelet can be manipulated in two ways, translation and scaling. Mathematically, a wavelet can be denoted as:

$$\psi_{a,b}(x) = \frac{1}{\sqrt{a}}\psi\left(\frac{x-b}{a}\right), \qquad a > 0$$

where 'b' is location parameter and 'a' is scaling parameter. A function should be time limited if it has to be a wavelet. For a given scaling parameter a, we translate the wavelet by varying the parameter b. By choosing appropriate values for 'a' and 'b', small segments of a complicated form may be represented with higher resolution, while smooth sections can be represented with a lower resolution.

Generally wavelet transform is used as a tool to decompose functions or operators into diverse frequency components. The transform is computed generally at various locations of the signal and for various scales of the wavelet, thus filling up the transform plane. If the process is done in a smooth and continuous fashion then the transform is called Continuous Wavelet Transform (CWT). If the scale and position are changed in discrete steps, the transform is called Discrete Wavelet Transform (DWT). (Ramtin et al., 2012), (Maryam Nassser and Masoud Mohammadi, 2012)

Continuous wavelet transform is defined by the inner product of the function and basis wavelet,

$$CWT_f(a,b) = \frac{1}{\sqrt{a}}\int_{-\infty}^{\infty} f(x)\psi\frac{x-b}{a}dx$$

According to this equation for every (a,b), we have a wavelet transform coefficient, representing how much the scaled wavelet is similar to the function at location x= (b/a). The practical application of CWT is limited by the redundant and non-finite nature of the coefficients. These coefficients are obtained by the correlation of the function and the wavelet performed during the continuous translation and scaling of the wavelet. Discretization is therefore resorted to, the time scale plane being discretized into grid nodes at which the CWT is performed. The generation of fast algorithms calls for the development of discrete wavelets, which are usually part by part continuous functions.

3. Generalized Algorithm

The fault diagnosis methodology may be divided into the following distinct steps.

1. Formulation of a model of the CUT which is a three phase single level VSI in this case.
2. Application of the wavelet transforms for the various fault condition as well as fault free condition.
3. Building a fault dictionary by extracting the standard deviation of the transform coefficients.
4. Identifying of fault.

4. Circuit under Test - Three Phase Single Level VSI

To test the performance of this technique for fault diagnosis, we choose a three phase single level IGBT based VSI as shown in Figure 1. The circuit was modelled using MATLAB. The model consists of a 400V DC and a series RLC circuit as an arbitrary load. A resistance of 1000Ω and an inductance of 5H and a capacitance of 0.006F were assumed in the construction of the model. The necessary gating signals to the thyristor switches have been provided by the pulse generators operating at 50% duty cycle.

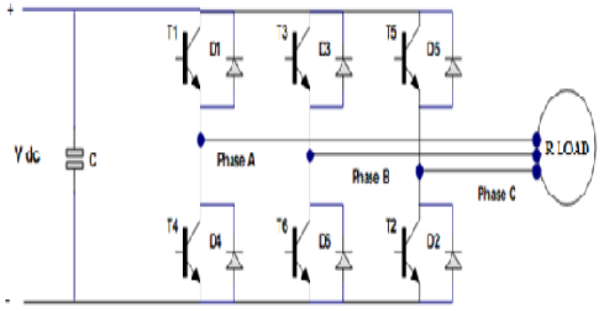

Figure 1. Three phase single level VSI

The open circuit and short circuit fault are simulated by the circuit model as shown in the Figure 2 (Open Circuit fault - OF) and in the Figure 3 (Short Circuit fault -SF).

The former fault is simulated by removing the gating pulse for the semiconductor switch. This is done by disconnecting the function generator. This model is based on the assumption of ideality of the semiconductor that may not conduct in the absence of a gate signal, thus acting as an open circuit. While the latter fault is simulated by bypassing the IGBT switch.

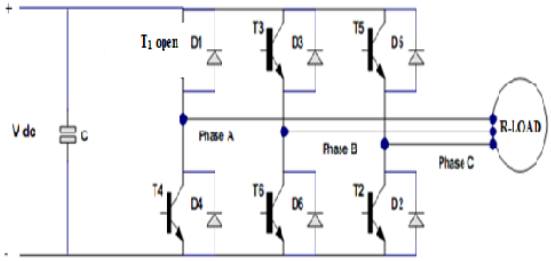

Figure 2. Open Circuit Fault-IGBT1 is assumed to be open

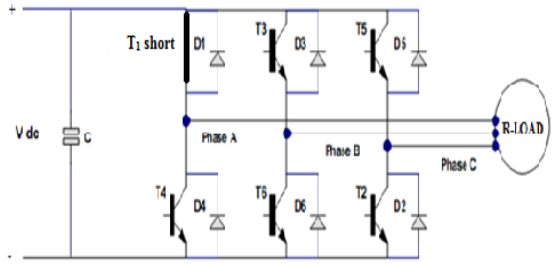

Figure 3. Short Circuit Fault- IGBT1 is assumed to be short circuited

The output voltage waveform, pertaining to the phase A, phase B and phase C corresponding to open circuit fault at IGBT4, designated OF4, has been provided in Figure 4, Figure 5 and Figure 6 respectively.

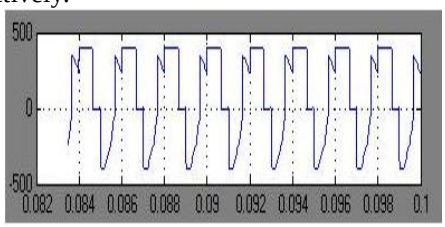

Figure 4. Output voltage waveform for phase A for fault OF4

5. Signature Extraction

In order to build the fault dictionary, the signatures for each fault condition as well as for the fault free condition has to be extracted. This utilizes the statistical analysis of transform coefficients. In this paper single as well as double faults have been considered. However, this technique can be extended to higher degree of faults without any change in the methodology.

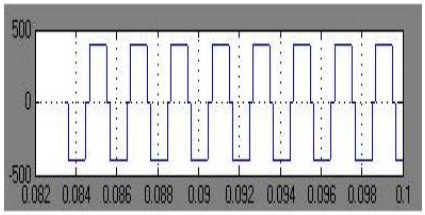

Figure 5. Output voltage waveform for phase B for fault OF4

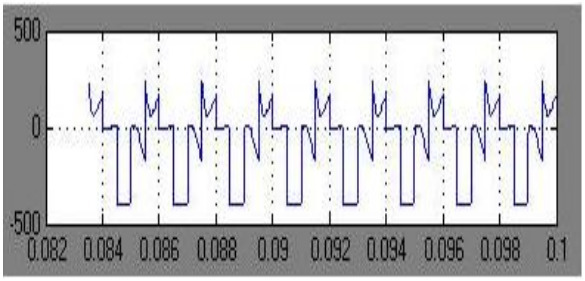

Figure 6. Output voltage waveform for phase C for fault OF4

In a three phase single level VSI circuit consisting of 6 thyristors, there is a possibility for the occurrence of 6 open circuit single faults and 15 open circuit double faults. Similarly, there is a possibility for the occurrence of 6 short circuit single faults and 15 short circuit double faults [Kastha and Bose, 1994]. Owing to the aberration in the output due to the short circuit of the voltage source, the cases of shot circuit double faults in which both the faults occur in switches belonging to the same arm. The absence of any output voltage in the fault free legs leads to the failure of any attempt to perform wavelet transform.

The output voltage of each phase is analyzed using Wavelet Toolbox in MATLAB. The choice of the mother wavelet used is primarily influenced by the occurrence of redundancies in the signatures. The wavelets which do not pose redundancy problems are further prioritized based upon the efficiency of the classifier when operated in tandem. The performance of each wavelet for individual CUTs differs thereby postulating a detailed performance analysis of the various wavelets. In this paper, however, emphasis has been laid on establishing the simplicity of the approach without a compromise on accuracy. After a detailed analysis, the Symlet-2 wavelet qualified as the wavelet of choice. The wavelet was employed at fifth level of detail. This is highly important because the level of detail has a marked impact on the efficiency of the classifier. Higher the level of detail chosen for extraction, greater is the efficiency. Thus the choice of level of detail involves a trade-off between efficiency and simplicity.

The transformation is being followed by statistical analysis. The standard deviation (SD) was chosen as the statistical parameter. This is due to the fact that SD spans a finite positive spectrum with adequate margin between the potential signatures for various faults. Thus the fault dictionary is being framed by tabulating the SD extracted for all three phases for the various test fault conditions. This fault dictionary is then used for fault identification.

The waveforms shown in Figure 4 through Figure 6 are then loaded into the wavelet toolbox followed by their statistical analyses. The wavelet transforms for phase A, phase B and phase C are shown in Figure 7, Figure 8 and Figure 9. The statistical analysis tool outputs are displayed for the three phases in Figure 10, Figure 11 and Figure 12 in the respective order.

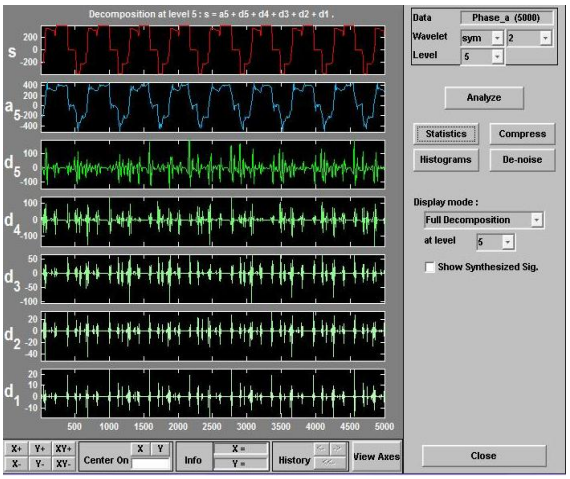

Figure7. Wavelet transform for phase A for fault OF4

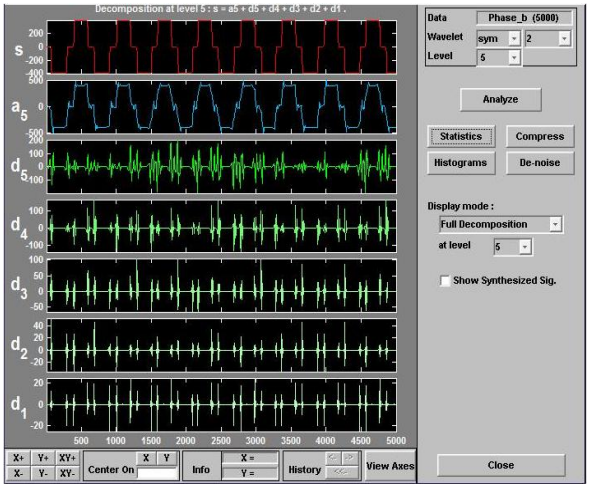

Figure 8. Wavelet transform for phase B for fault OF4

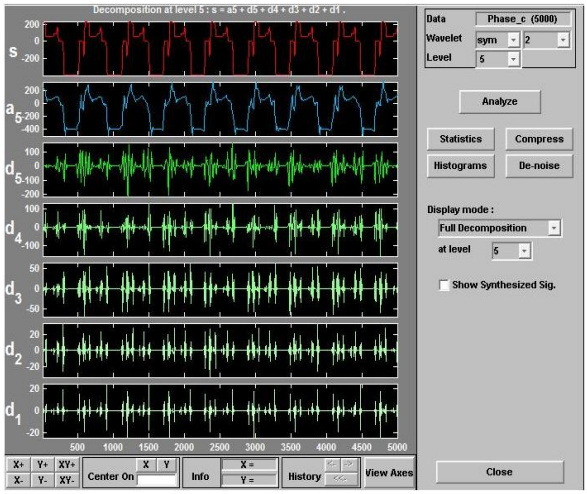

Figure9. Wavelet transform for phase C for fault OF4

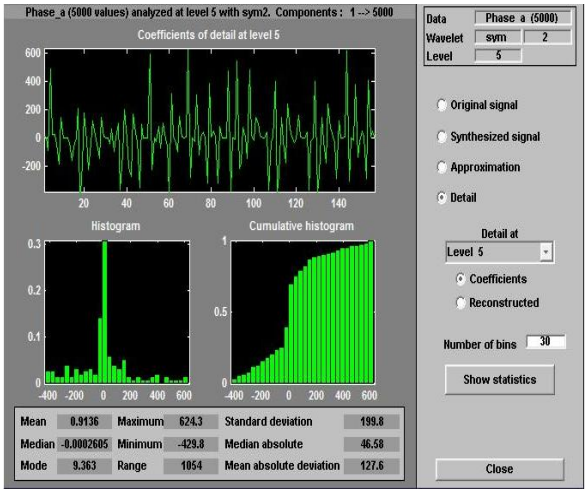

Figure10. Statistical analysis of wavelet transform for phase A for fault OF4

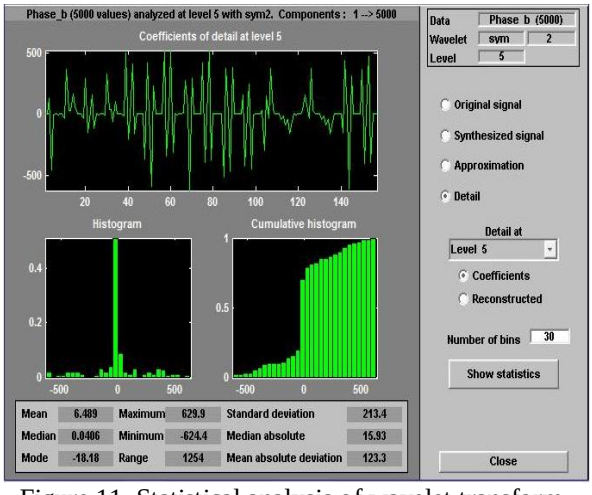

Figure 11. Statistical analysis of wavelet transform for phase B for fault OF4

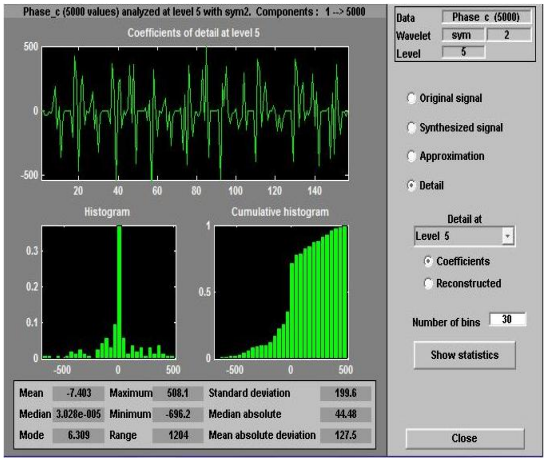

Figure 12. Statistical analysis of wavelet transform for phase C for fault OF4

6. Fault Dictionary

The standard deviations extracted for all the three phases for the various test faults considered was then tabulated. Table 1 and Table 2 represent the fault dictionary developed for open circuit faults and short circuit faults respectively. This fault dictionary is developed for the circuit three phase single levels VSI.

Table 1. Open Circuit Fault dictionary for voltage source inverter

Fault ID	Faulty Component	SD for phase A	SD for phase B	SD for phase C
FF	FF	186.70	186.60	186.40
OF1	T1	202.60	213.50	205.90
OF2	T2	214.40	206.80	185.10
OF3	T3	201.20	188.10	192.00
OF4	T4	199.80	213.40	196.60
OF5	T5	231.50	213.50	216.30
OF6	T6	180.50	199.30	210.00
OF7	T1, T2	200.10	205.00	173.40
OF8	T3, T4	181.30	206.40	201.40
OF9	T1, T4	170.00	233.40	184.90
OF10	T1, T6	168.50	210.90	194.20
OF11	T2, T3	232.70	199.90	247.00
OF12	T2, T5	209.00	207.70	166.90
OF13	T3, T5	216.30	193.40	190.70
OF14	T4, T5	199.40	200.10	179.30
OF15	T4, T6	203.50	211.50	175.30

Table 2. Short Circuit Fault dictionary for voltage source inverter

Fault ID	Faulty Component	SD for phase A	SD for phase B	SD for phase C
SF1	T1	176.10	238.60	161.10
SF2	T2	249.90	177.60	177.10
SF3	T3	164.40	181.00	244.80
SF4	T4	172.80	230.10	151.80
SF5	T5	253.60	180.00	178.30
SF6	T6	174.20	186.30	255.00

7. Result

The five inputs corresponding to the faults OF1, OF2, OF14, SF3 and SF4 were given to the FIS. After simulation of faults, the corresponding wavelet transform coefficients were provided to generate the fault identification. The system was capable of analysing the faults. To check the capability and reliability of the system, two test inputs OF14 (open fault) and SF6 (short fault) were tested. Table 3 represents the results obtained.

Table 3. Fault dictionary for voltage source inverter

Switching States						Classifier Inputs			Fault ID
T1	T2	T3	T4	T5	T6	SDa	SDb	SDc	
N	N	N	N	N	N	186.7	186.6	186.4	FF
O	N	N	N	N	N	202.6	213.5	205.9	OF1
N	O	N	N	N	N	214.4	206.8	185.1	OF2
N	N	N	O	O	N	199.4	200.1	179.3	OF14
N	N	S	N	N	N	164.4	181.0	244.8	SF3
N	N	N	S	N	N	172.8	230.1	151.8	SF4
N	N	N	O	O	N	199.4	200.1	179.3	OF14
N	N	N	N	N	S	174.2	186.3	255.0	SF6

N-Normal OF-Open Fault SF-Short Circuit Fault FF-Fault Free

8. Validation

The single phase multilevel inverter circuit has been chosen as circuit for validation of the proposed methodology. The circuit is shown in Figure 13. The five level inverter circuits consist of two 24V Separate DC Sources (SDCS) and R load. The gating signals to the IGBT switches have been provided by sinusoidal PWM with a modulation index of 0.9/1.0. A method for operating cascaded multilevel inverters when one or more power H-bridge switches is damaged has been proposed in (Khomfai and Tolbert, 2005). The fault diagnosis of multilevel inverter using neural network has been proposed in (Rodriguez et al., 2005). The output voltages of a multilevel inverter can also be used to diagnose the fault types (open circuit) as depicted in Figure 15 and Figure 16. The output voltage waveform of fault free, single fault and double condition are shown in Figure 14, Figure 15 and Figure 16 respectively.

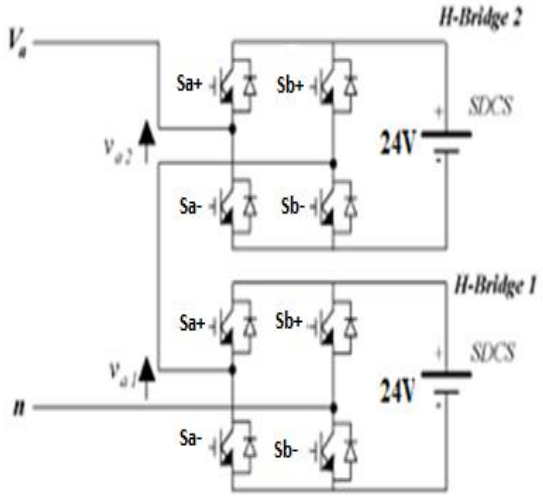

Figure 13. Single phase multilevel inverter

In order to build the fault dictionary, the signatures for fault free, single fault as well as double fault condition has to be extracted. All the three output voltages are analyzed using Wavelet Toolbox in MATLAB.

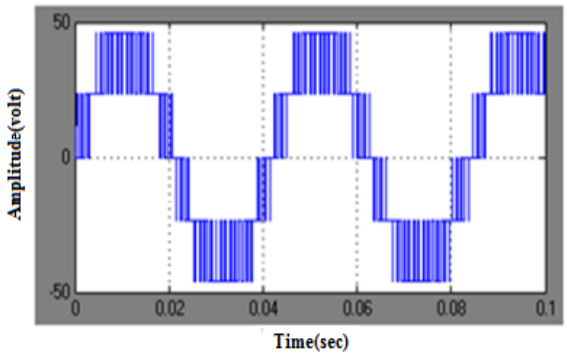

Figure 14. Output voltage waveform for fault free condition

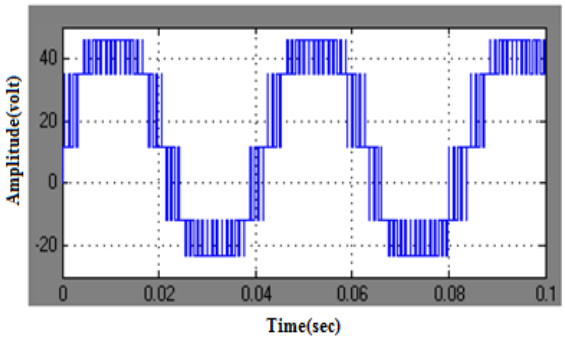

Figure 15. Output voltage waveform for fault Sa+

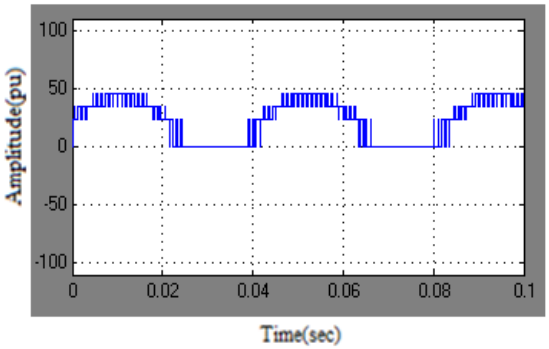

Figure 16. Output voltage waveform for fault Sa+ and Sa-

The waveforms shown in Figure 14 through Figure 16 are then loaded into the wavelet toolbox followed by their statistical analyses. The wavelet transforms for fault free, single fault and double fault are shown in Figure 17, Figure 18 and Figure 19. The statistical analyses for the above faults are displayed in Figure 20, Figure 21 and Figure 22 respectively. From the statistical analysis, the standard deviation values for the various fault conditions are tabulated. Table 4, represents the fault dictionary developed for fault free, single fault and double fault. From Table 4, it is found that the standard deviation values are distinct for each type of fault. By using a suitable classifier the type of fault and the faulty switch can easily be detected.

10. Conclusion

The fault detection methodology proposed in this paper uses both wavelet transformation and statistical analysis to diagnose faults in power electronic circuits. Here wavelet transformation technique has been utilized to transform output voltage signals to derive parameters for fault signature generation. Further wavelet transformation gives a better performance when transient signals are considered. The use of statistical analysis has further improved the robustness of the system. Thus the system represented is reliable and capable of identifying the faults in an efficient manner using the fault dictionary. The proposed method is characterized by its accurate fault identification. The effectiveness of the method has been explained using the voltage source inverter as a test circuit. The results exhibited that the fault signatures were distinct. This method has also been validated by considering a single phase multilevel inverter circuit which provided similar results for future. A Fuzzy or neural system can suitably be designed as a fault classifier, which will make the fault identification easier and simple. (Ananthamoorthy and Baskaran, 2012) (Pandian and Dhanasekaran, 2013).

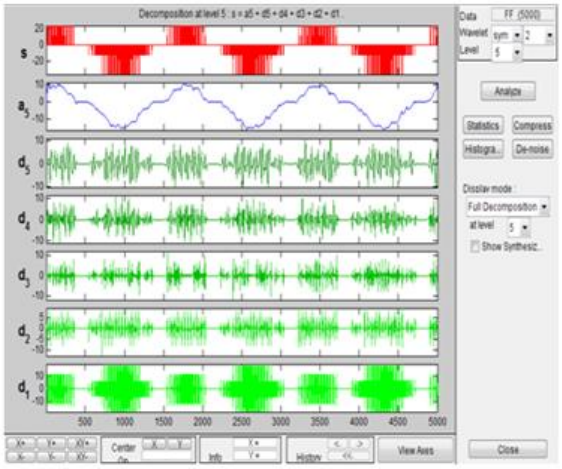

Figure 17. Wavelet transform for fault free FF

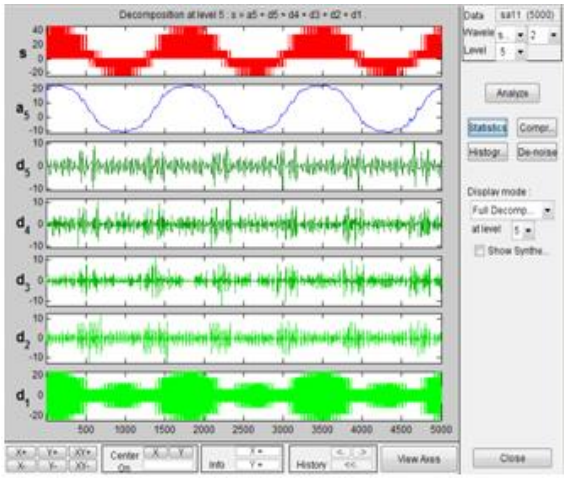

Figure 18. Wavelet transform for single fault Sa+

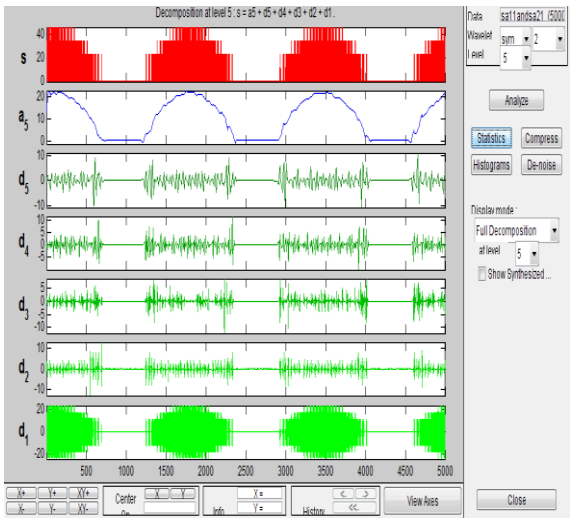

Figure 19. Wavelet transform for Double fault Sa+ and Sa-

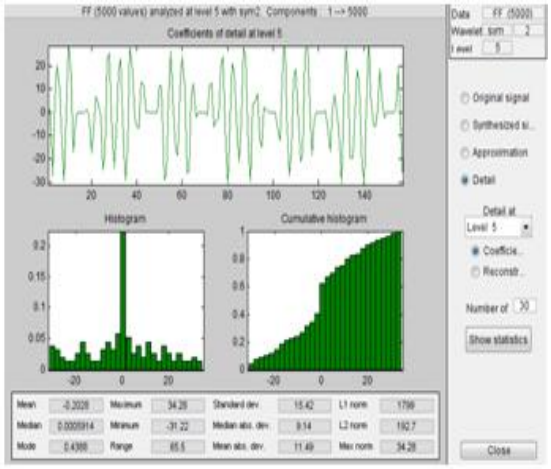

Figure 20. Statistical analysis of wavelet transform for fault free FF

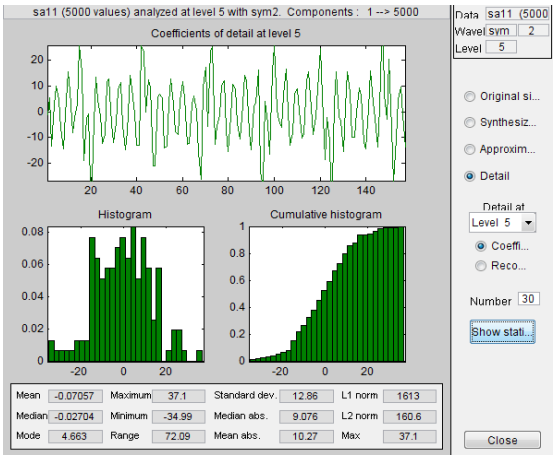

Figure 21. Statistical analysis of wavelet transform for Single fault Sa+

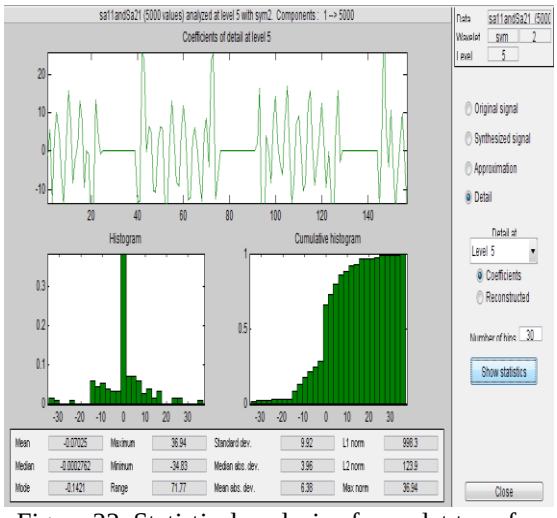

Figure 22. Statistical analysis of wavelet transform for Double fault Sa+ and Sa-

Table 4. Fault Dictionary for Multi Level Inverter

Fault type		Bridge 1				Bridge 2				Standard deviation
Fault free	1	-	-	-	-	-	-	-	-	18.10
Single	1	Sa+	-	-	-	-	-	-	-	12.86
	2	-	Sa-	-	-	-	-	-	-	12.84
	3	-	-	-	-	-	-	Sb+	-	15.77
	4	-	-	-	-	-	-	-	Sb-	15.75
Double	1	Sa+	Sa-	-	-	-	-	-	-	09.14
	2	-	Sa-	Sb+	-	-	-	-	-	10.43
	3	-	Sa-	-	Sb-	-	-	-	-	10.53
	4	Sa+	-	-	Sb-	-	-	-	-	10.47
	5	-	-	-	-	Sa+	Sa-	-	-	14.99
	6	-	-	-	-	-	Sa-	Sb+	-	12.81
	7	-	-	-	-	-	Sa-	-	Sb-	14.99
	8	-	-	-	-	Sa+	-	-	Sb-	12.29
	9	Sa+	-	-	-	Sa+	-	-	-	09.92
	10	Sa+	-	-	-	-	Sa-	-	-	09.14
	11	-	Sa-	-	-	-	-	Sb+	-	09.66
	12	-	Sa-	-	-	-	-	-	Sb-	09.14

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References

[1] M. Rozailan Mamat, M. Rizon, and M.S. Khanniche, "Fault detection of 3-phase vsi using wavelet- fuzzy algorithm", American Journal of applied Sciences, 2006; 1642-1648.

[2] K.Rothenhagen and F.W. Fuchs, "Performance of diagnosis methods for IGBT open circuit faults in three phase voltage source inverters for AC variable speed drives", in Proceedings European Conference on Power Electronics Application, Dresden, Germany, 2005:1-10.

[3] A.C. Renfrew and J.X. Tian, "The use of a knowledge-based system in power electronic circuit fault diagnosis", Fifth European Conference on Power Electronics and Applications, 1993; 7:57-62.

[4] J. W. Bandler and A. E. Salama, "Fault diagnosis of analog circuits", Proc. IEEE, 1985; 73(8): 1279–1325.

[5] Tadeusiewicz, M., Halgas, S., and Korzybski, M., "An algorithm for soft-fault diagnosis of linear and nonlinear circuits", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 2002; 49(11):1648-1653.

[6] Dubois, Prade, "Fuzzy sets and systems", Academic Press, New York, Nov 1980.

[7] S. Abramic, W. Sleszynski, J. Nieznanski,and H. Piquet, "A diagnostic method for on-line fault detection and localization in vsi-fed drives", 10th European Conference on Power Electronics and Applications, Toulouse, France , 2003.

[8] A. Mckeon and A. Wakeling, "Fault diagnosis in analogue circuit using AI technique", IEEE Int. Test Conf., 1989:118–123.

[9] Gertler,J.J, " Fault detection and diagnosis in engineering systems", Marcel Dekker, New York, 1998.

[10] Ramtin Sadeghi, Reza Sharifian Dastjerdi, Payam Ghaebi Panah, Ehsan Jafari. "Automatic Detection and Positioning of Power Quallity Disturbances using a Discrete Wavelet Transform". Life Sci J 2012; 9(4):3481-3486.

[11] Maryam Nassser and Masoud Mohammadi. "Condition Monitoring using Wavelet Transform and Fuzzy Logic by Vibration Signals". Life Sci J 2012;9(4):5680-5685

[12] D.Kastha, B.K. Bose, "Investigation of fault modes of voltage -fed inverter system for induction motor drive", IEEE Transaction on Industrial Applications, 1994; 30(4):1028-1037.

[13] Khomfai S. and Tolbert L.M, 'Fault diagnosis system for a Multilevel Inverters Using a Neural Network', in IEEE Transaction, 2005:1455-1460.

[14] J. Rodriguez, P. W. Hammond, J. Pontt, R. Musalem, P.Lezana, and M.J. Escobar,"Operation of a medium-voltage drive under faulty conditions,"IEEE Trans. Ind. Electron., 2005;52(4):1080–1085.

[15] Ananthamoorthy.N.P, Baskaran. K. "Performance Analysis of PMSM Drive Using Intelligent Hybrid Fuzzy Controller". Life Sci J 2012; 9 (1s):112-120.

[16] Pandian. A, Dhanasekaran. R. Torque Ripple Minimization in Direct Torque Control of Induction Motor using Fuzzy Technique. Life Sci J 2013; 10(1s):133-139] (ISSN: 1097-8135).

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